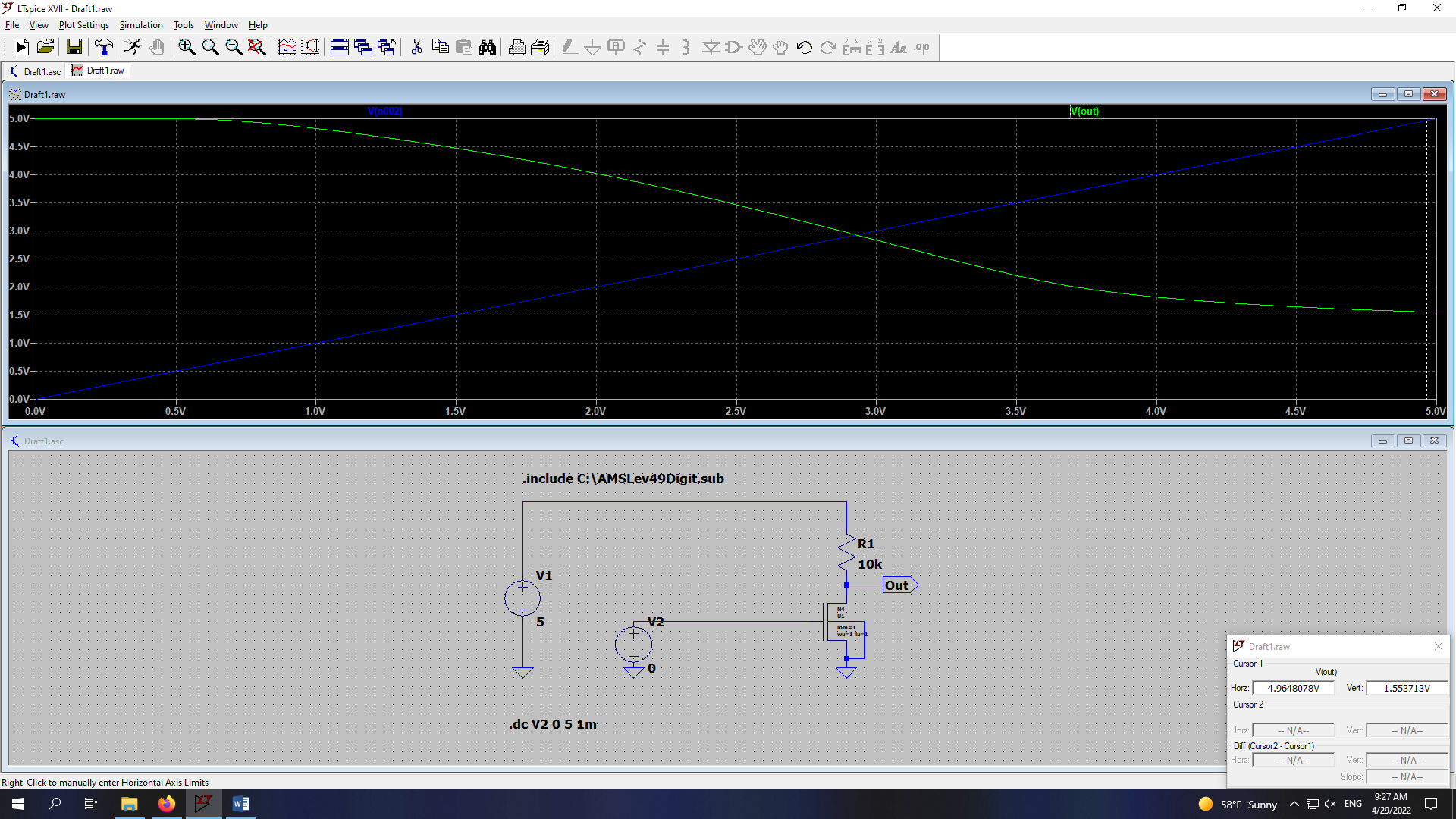
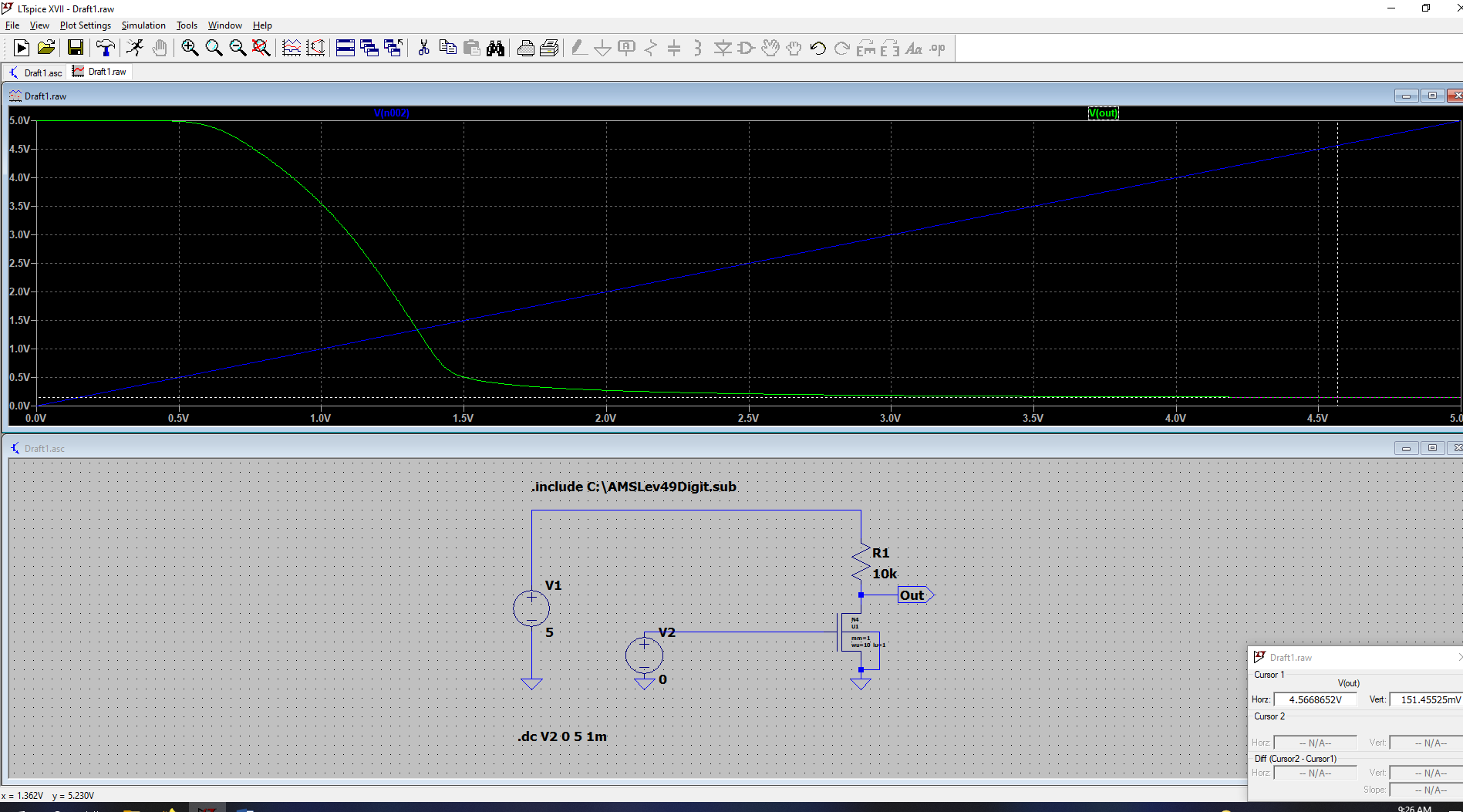
**Measurement Task**

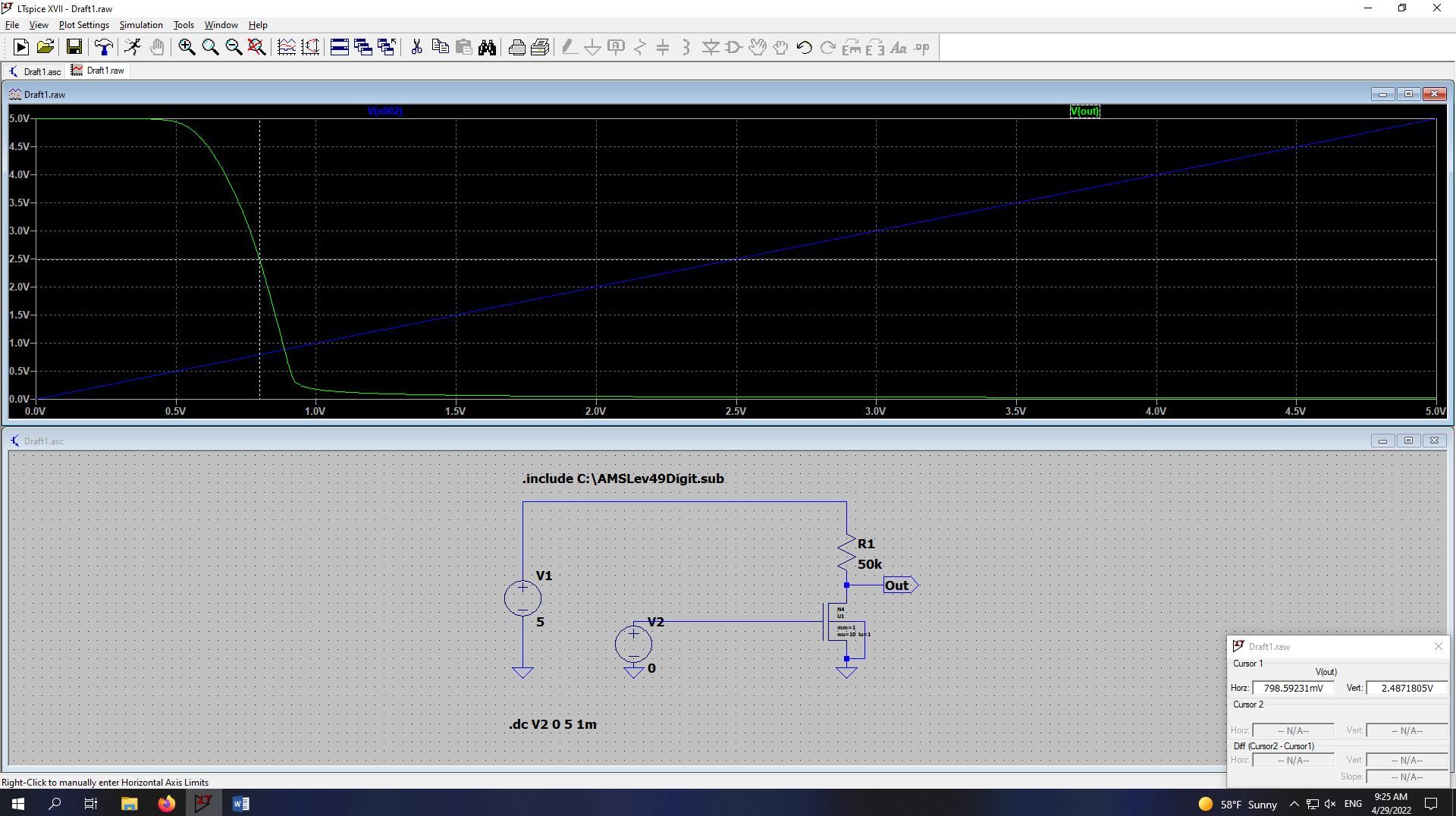
Ideally, when Vgs < Vt, the output will be VDD. when the input Vgs >= VT, the output should go from VDD to 0 immediately.



the problem is, the final value doesn’t go to 0, it goes to only around 1.5V. we can change this by change the dimension size of transistor. we will decrease it by increase the size of the width, we changed the width to 10

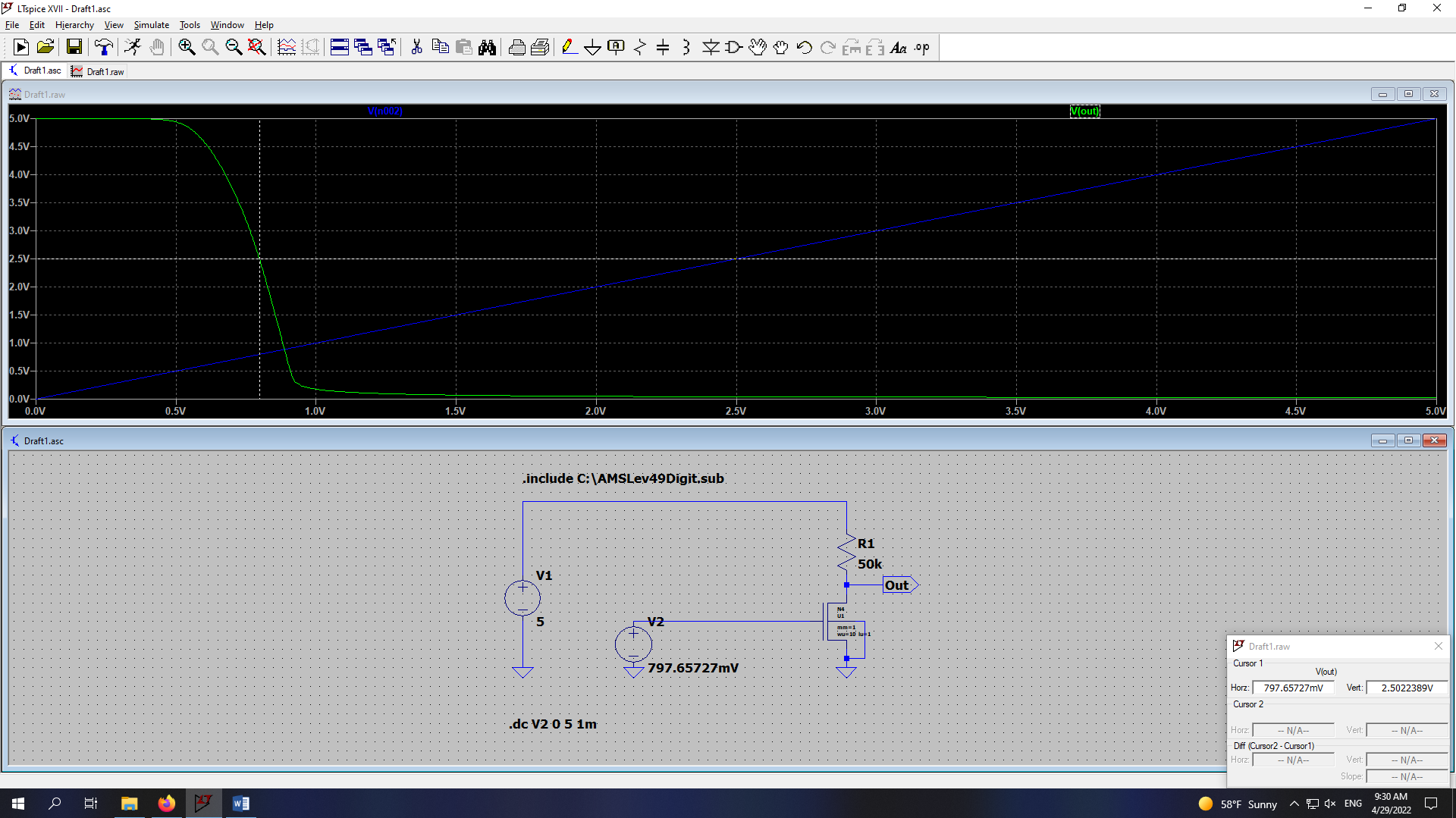


Here we can decrease the output offset error further by increase the value of R1. I will increase it to 50k

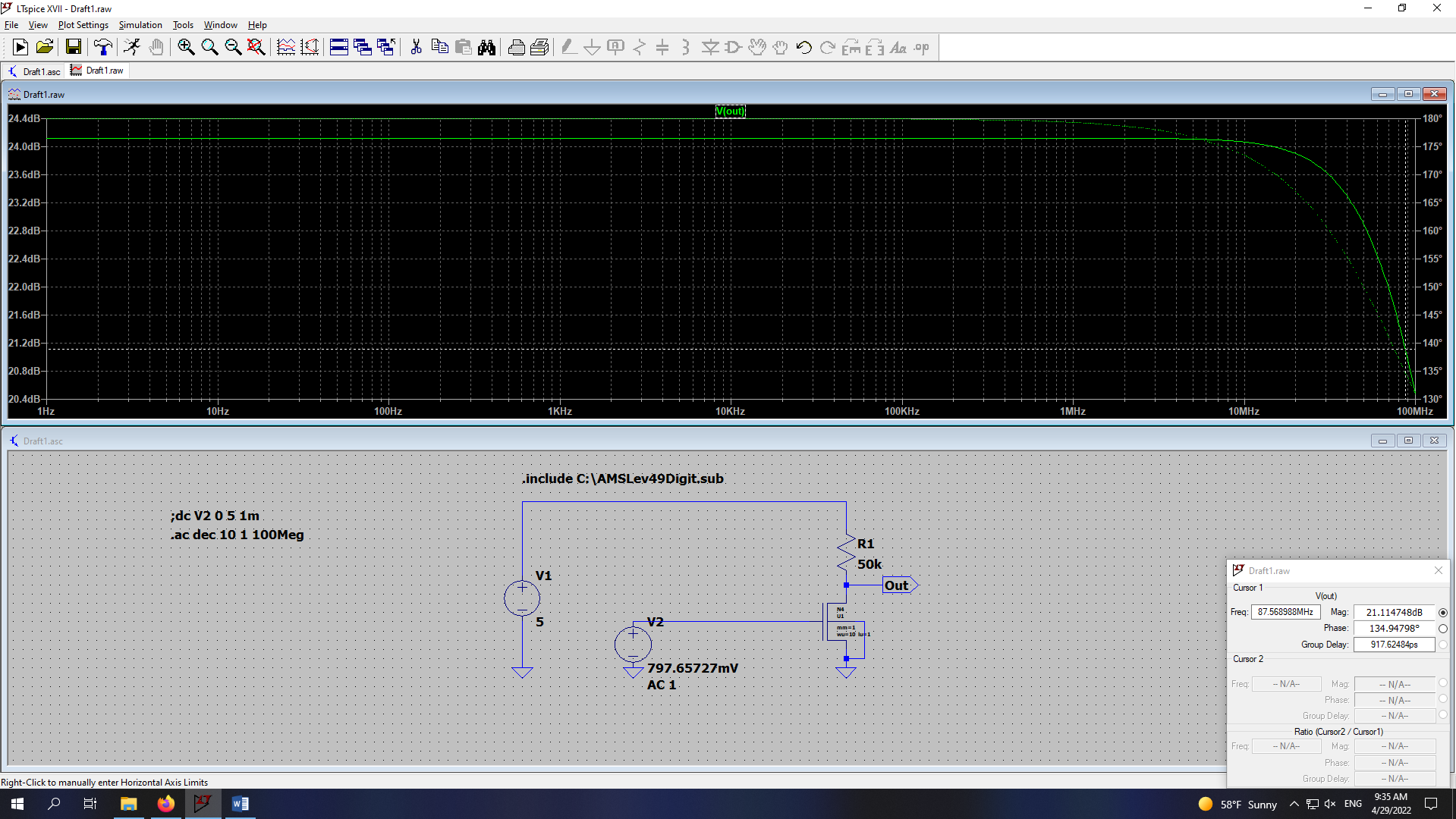


**finding the operating point**

we found the operating point where the output is half of the power supply, and at this point the 0.676V.



we can check the cut-off frequency and the amplification on the bode plot

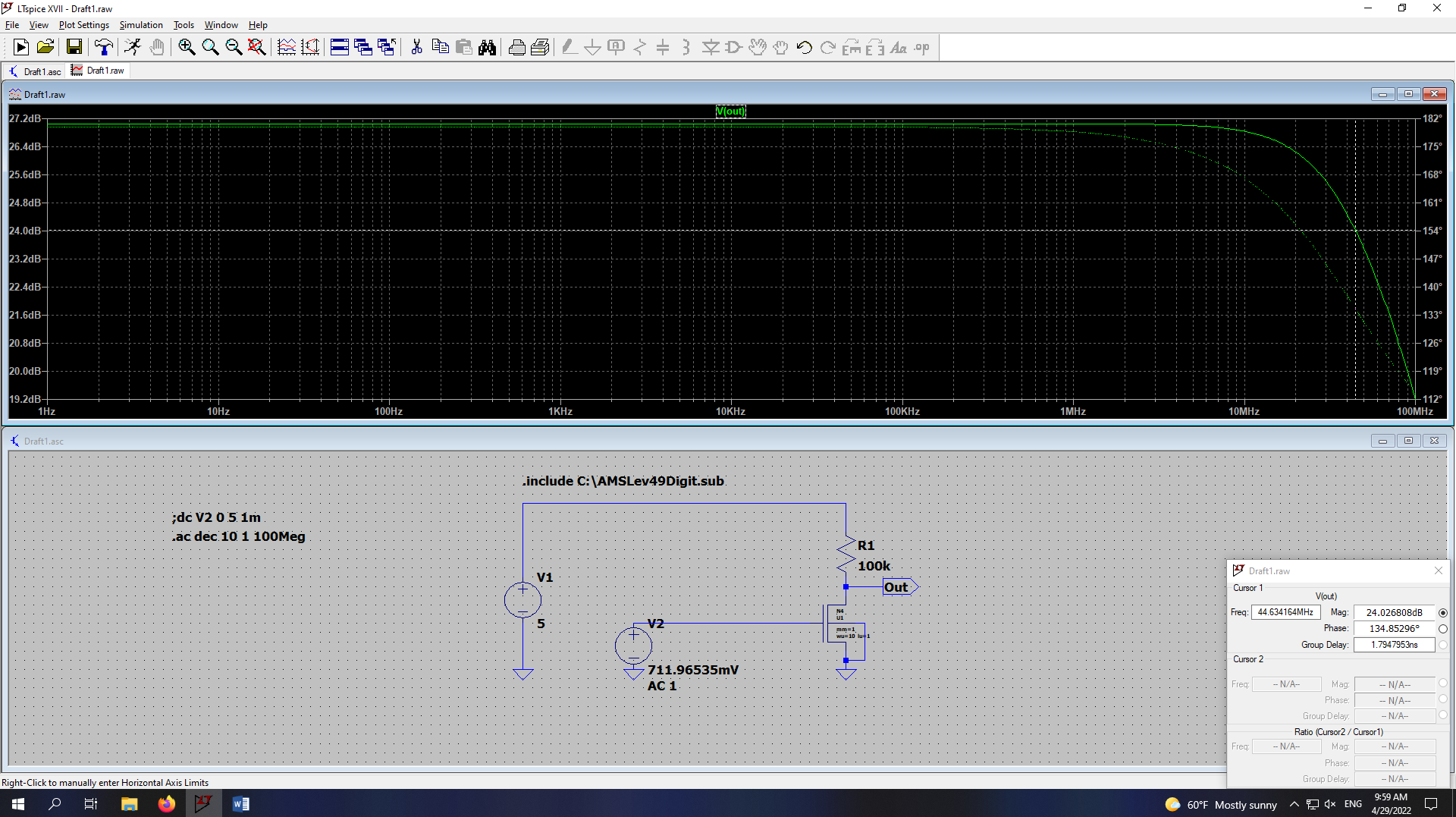


we can get the cut-off frequency when amplitude is decreased by 3dB

we have the cut-off frequency is 87.568 MHz. (in this case V2 and the operating point is 797.56mV)

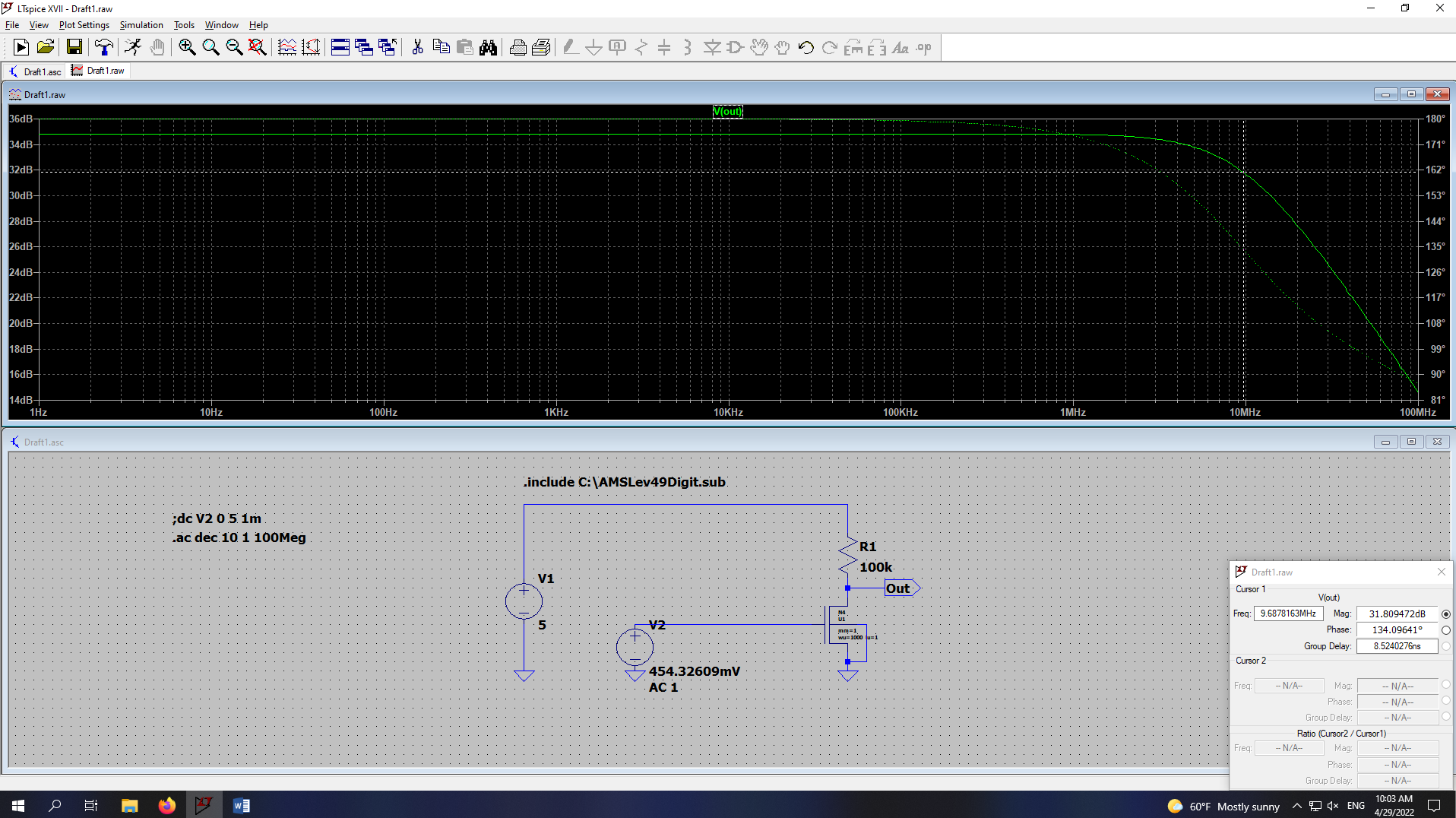
**Increase the amplification**

we can further increase the amplification by either increase the conductance of the transistor which will be the dependent source in AC simulation or increase the Rload. we will increase the Rload to 100k



we see that now the cut-off frequency is 44.63 MHz. I also changed the V2 based on the operating point. which V2 = 711.9535mV

we can further increase the amplification by increase the conductance by increase the width of nMOS (MAX 1000), I will increase it to 1000



in this case we found that the cut-off frequency is 9.68MHz and I did changed the V2 to the new operating point which is 454.32mV